

WHAT IS CLAIMED IS:

1. A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

5 a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer located upon the first oxide layer;

a second oxide layer, located upon the high dielectric constant dielectric layer,

wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;

10 a control gate formed on the second oxide layer of the dielectric stacked layer;

and

a source/drain region located in the substrate on the two sides of the floating gate.

15 2. The flash memory structure as defined in claim 1, wherein a band gap value of the high dielectric constant dielectric layer is less than a band gap value of silicon oxide .

3. The flash memory structure as defined in claim 1, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8.

20 4. The flash memory structure as defined in claim 1, wherein the high dielectric constant dielectric layer is a single layer including one material selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

5. The flash memory structure as defined in claim 1, wherein the high dielectric constant dielectric layer is a layer including a mixed material any one selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and

TiO₂.

6. The flash memory structure as defined in claim 1, wherein the material of the high dielectric constant dielectric layer is stacked layer, each layer of the stacked layer including one selected from the group consisting of Al₂O₃, Y₂O₃, ZrSi_xO_y, HfSi_xO_y,

5 La₂O₃, ZrO₂, HfO₂, Ta₂O₅, Pr₂O₃ and TiO₂.

7. A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

10 a high dielectric constant dielectric layer located upon the first oxide layer,

wherein, together with the oxide layer, a dielectric stacked layer is formed;

a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and

15 a source/drain region located within the substrate on the two sides of the floating gate.

8. The flash memory structure as defined in claim 7, wherein a band gap value of the high dielectric constant dielectric layer is greater than a band gap of silicon oxide.

9. The flash memory structure as defined in claim 7, wherein a band gap value of the high dielectric constant dielectric layer is equivalent to a band gap of silicon
20 oxide.

10. The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer is a single layer including one material selected from the group consisting of Al₂O₃, Y₂O₃, ZrSi_xO_y, HfSi_xO_y, La₂O₃, ZrO₂, HfO₂, Ta₂O₅, Pr₂O₃ and TiO₂.

11. The flash memory structure as defined in claim 7, wherein the high dielectric

constant dielectric layer includes a mixed material selected from any one of the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

12. The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer is a stacked layer, each layer of the stacked layer including one
5 selected from the group consisting of Al_2O_3 , Y_2O_3 , ZrSi_xO_y , HfSi_xO_y , La_2O_3 , ZrO_2 , HfO_2 , Ta_2O_5 , Pr_2O_3 and TiO_2 .

13. A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

10 an Al_2O_3 layer located upon the floating gate;

a control gate located upon the Al_2O_3 layer; and

a source/drain region located within the substrate on the two sides of the floating gate.